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Docket No.: 50006-070

## PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

## Application of

Jiro MATSUFUSA, et al.

Application No.: 09/620,718

Filed: July 20, 2000

For: SEMICONDUCTOR DEVICE HAVING TEST MARK

Customer Number: 20277

Confirmation Number: 3318

Group Art Unit: 2814

Examiner: G. Peralta

# TRANSMITTAL OF APPEAL BRIEF

**Mail Stop Appeal Brief - Patents**  
**Commissioner for Patents**  
**P.O. Box 1450**  
**Alexandria, VA 22313-1450**

Sir:

Submitted herewith in triplicate is Appellants' Appeal Brief in support of the Notice of Appeal filed September 9, 2003. Please charge the Appeal Brief fee of \$330.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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**APPEAL BRIEF**

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Commissioner for Patents  
P.O. Box 1450  
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Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed September 9, 2003.

I. **REAL PARTY IN INTEREST**

The real party in interest is Mitsubishi Denki Kabushiki Kaisha.

II. **RELATED APPEALS AND INTERFERENCES**

Appellants are unaware of any related appeals and interferences.

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### III. STATUS OF CLAIMS

Claims 1-8 are pending in this application and have been finally rejected. It is from the final rejection of claims 1-8 that this Appeal is taken.

### IV. STATUS OF AMENDMENTS

No amendments to the claims have been filed subsequent to the Final Office Action dated May 21, 2003.

### V. SUMMARY OF INVENTION

The present invention addresses and solves the problem of cracking in a conventional test mark (page 2 of Appellants' disclosure). The test mark of the prior art includes a first insulating layer 22 made of BPTEOS formed over a substrate 21 and a second insulating layer 23 made of TEOS formed over the first insulating layer 22. A recess or concave 24, as the test mark, is formed in both the TEOS and BPTEOS layers 22, 23 (page 2, lines 2-11). The recess 24 also has a square configuration (page 2, line 13; Fig. 14A). The cracks occur when the BPTEOS layer 22 is deformed, by sintering for example, while at the same time the TEOS layer 23 is only slightly deformed (page 2, lines 16-19). The differences between how the BPTEOS layer 22 and the TEOS layer 23 react to heat creates stress that result in a crack 27 in the BPTEOS layer 22 that extends outwardly from a corner of the recess 24 (page 2, lines 19-21). This crack 27 can disadvantageously destroy other semiconductor elements formed on the substrate 21 or other test marks. Therefore, there was a need for an improved test mark structure that minimized the occurrence of cracks in the test mark.

According to the present invention, the above crack problem is solved by forming a test mark that includes, in part, metal layer 6 on a first TEOS layer 2 and opposing a corner of a recess 4, as recited in independent claim 1. If, as illustrated in Fig. 1A, a crack 7 forms in a second TEOS layer 3 adjacent a corner of the recess 4, the crack 7 will terminate at the metal layer 6 (page 9, lines 15-18). Thus, the crack 7 will not extend beyond the metal layer 6 and adversely affect semiconductor elements formed on the substrate 1 or other test marks. The present invention, thus, constitutes an improvement over conventional test marks by providing a structure (i.e., the metal layer) that halts crack propagation from the test mark.

## VI. ISSUES

### A. The Rejection:

1. Claims 1-8 were rejected under 35 U.S.C. § 103 for obviousness based upon Appellants' Admitted Prior Art in view of Chen et al.

### B. The Issue Which Arises In This Appeal And Requires Resolution By The Honorable Board of Patent Appeals And Interferences (The Board) Is:

1. Whether claims 1-8 are unpatentable under 35 U.S.C. § 103 for obviousness based upon Appellants' Admitted Prior Art in view of Chen et al.

## VII. GROUPING OF CLAIMS

The appealed claims do not stand or fall together as a group. Claims 1-3 and 6-7 stand or fall together as a group with claim 1. Claims 4, 5 and 8 each stand or fall alone.

VIII. THE ARGUMENT

**The Rejection of Claims 1-8 under 35 U.S.C. § 103 for Obviousness based upon Appellants' Admitted Prior Art (hereinafter Admitted Prior Art) in view of Chen et al., U.S. Patent No. 6,118,185 (hereinafter Chen)**

In the Final Office Action dated May 21, 2003, the Examiner asserted that the Admitted Prior Art teaches all of the claimed limitations in independent claim 1 except for the following feature: "a metal layer formed on said first TEOS layer and opposing a corner of said recess."

The Examiner then asserted the following on page three of the Office Action:

Chen et al. teaches in fig. 14 a semiconductor device having a semiconductor substrate, that has a recess configuration on which a metal layer 92 is formed on an insulating layer 17 and opposing to the corner of the recess 3 which has a substantially square or rectangular configuration, wherein there is an outer metal layer formed outside of the metal layer 83 so that the outer metal layer opposes the corner of the alignment mark, and wherein the metal layer 83 is embedded in the insulating layer that extends between the top and bottom surfaces of the substrate, wherein the metal layers are used for the disclosed intended purpose of providing a structure that makes the mark on the wafer easier to identify and to eliminate the tendency for the outer box to be broken in critical places.

In response, Appellants submit that the Examiner's characterization of Chen is without factual basis, and the Examiner's asserted benefits for modifying the Admitted Prior Art in view of Chen are not persuasive. For these reasons, as will be discussed in more detail below, Appellants respectfully submit that one having ordinary skill in the art would not have been motivated to modify the Admitted Prior Art in view of Chen so as to arrive at the claimed invention.

The Examiner's assertion that Fig. 14 of Chen discloses "a semiconductor substrate that has a recess configuration" (emphasis added) is without a factual basis. Although the Examiner

did not initially identify what feature allegedly disclosed the claimed recess, the Examiner later identified feature 3 as corresponding to the recess. Since Fig. 14 is a plan view of the structure, it is difficult to determine from this figure whether or not feature 3 is recessed within the insulating layer 17. Upon reviewing Chen, Appellants note that feature 3 is described in column 1, lines 29 as being a smaller box and inside the outer box 2. Also, in describing Figs. 5a, 5b in column 2, lines 25-26, Chen states that a photoresist pattern 53 corresponds to the inner box. Finally, in describing Figs. 12a, 12b, Chen states that a photoresist pattern 123 corresponds to the inner box. Thus, one having ordinary skill in the art would consider feature 3 in Fig. 14 to be an "inner box," as that term is used by Chen, and understand that the inner box corresponds to a photoresist pattern formed above the insulating layer 17. Therefore, the Examiner's assertion that the inner box 3 of Chen is a recess in the insulating layer 17 is without factual basis.

This misinterpretation of the teachings of Chen underscores the Examiner's failure to appreciate the differences between the test mark of the Admitted Prior Art and the box-in-box structure of Chen and why these differences would preclude one having ordinary skill in the art from arriving at the Examiner's proposed combination. As disclosed in Fig. 14 of the Admitted Prior Art and described in page 2 of Appellants' specification, a recess 24 is formed in both the TEOS and BPTEOS layer 22 and 23. The recess 24 acts as the "test mark" and is not disclosed as being used in combination with any other feature.

In contrast, Chen teaches an improvement to a box-in-box configuration. Chen's admitted prior art, as shown in Fig. 1a, teaches an inner box 3 that is used in combination with a single outer box 2. Chen's improvement, as shown in Fig. 14, replaces the single outer box 2 with a

series of concentric ridges 83. Although not explained in detail by Chen, the concept behind the box-in-box configuration is that one box (i.e., the outer box 2) is formed during one series of processing steps and the second box (i.e., inner box 3) is formed during a subsequent series of processing steps. By comparing the position of the outer box 2 to the position of the inner box 3, an operator can determine whether or not the separate masks used in the two separate sequences of processing steps were properly aligned. The improvement proposed by Chen (i.e., series of concentric ridges 83) was to overcome problems that resulted in the continuity of the outer box 2 being broken (column 2, lines 34-39). By using a series of concentric ridges 83, even if one of the ridges 83 was broken, the other ridges 83 could remain continuous (column 4, lines 39-44).

The Examiner's asserted motivation for modifying the Admitted Prior Art in view of Chen is (i) "[to provide] a structure that makes the mark on the wafer easier to identify" and (ii) "to eliminate the tendency for the outer box to be broken in critical places." As to the Examiner's first asserted motivation (i.e., make the test mark easier to identify), one having ordinary skill in the art would not have been motivated to modify the Admitted Prior Art in this manner since even if the Admitted Prior Art were so modified, the Examiner's asserted benefit would not be obtained. Chau teaches that the improvement in the recognition of the box-in-box feature is to replace the single outer box 2 with a series of ridges 83. However, the Admitted Prior Art does not teach any feature comparable to the outer box 2 of Chau. Thus, one having ordinary skill would not have been motivated to replace a non-existent feature in the Admitted Prior Art with the ridges 83 of Chau in the manner suggested by the Examiner.

Furthermore, even if the ridges 83 in Chau were formed on the first TEOS layer 22 of the



Admitted Prior Art in the manner suggested by the Examiner, the asserted benefit of making the test mark easier to identify would not result. Assuming that ridges 83 were formed on the first TEOS layer 22 of the Admitted Prior Art, the next step in forming the test mark (i.e., recess 24) would be to form the second TEOS layer 23, and this second TEOS layer 23 would cover the first TEOS layer and the ridges 83. Finally, once the second TEOS layer 23 is formed, the Admitted Prior Art teaches etching through layers 22 and 23 to form the recess (page 2, lines 8-11 of Appellants' specification). Since the second TEOS layer 23 covers the ridges 83, the ridges 83 cannot improve the identification of the test mark because the ridges 83 are not visible. Therefore, the Examiner's asserted benefit of making the test mark easier to identify would not result, and thus, not motivate one having ordinary skill in the art to modify the Admitted Prior Art in view of Chen in the manner suggested by the Examiner.

The Examiner's second motivation (i.e., to eliminate the tendency for the outer box to be broken in critical places) suffers from one of the same problems as the first motivation. Specifically, the Admitted Prior Art does not teach any feature comparable to the outer box of Chen. As such, why would one having ordinary skill in the art be motivated to modify the outer box of the Admitted Prior Art to eliminate the tendency for the outer box to be broken when the outer box does not exist in the Admitted Prior Art? Therefore, for the reasons stated above, Appellants respectfully submit that one having ordinary skill in the art would not have been motivated to modify the Admitted Prior Art in view of Chen so as to arrive at the claimed invention.

Appellants also submit that claims 4, 5 and 8 each contain subject matter that is

separately patentable over the Examiner's proposed combination of the Admitted Prior Art in view of Chen. Claims 4, 5 and 8 are directed to the shape of the metal layer formed on the first TEOS layer. In the statement of the rejection, the Examiner did not identify where the Admitted Prior Art or Chen, either alone or in combination, teach or suggest these particular limitations. However, the Examiner did assert the following:

Furthermore, it would have been obvious to one of ordinary skill in the art to form the metal layer having a variety of shapes as it would not yield any unexpected result, and the purpose of a better identification of the test mark would be accomplished and the tendency for the outer box to be broken in critical places will be largely eliminated.

From this statement, it appears that the Examiner is asserting that since the Examiner's two asserted benefits would still result and Appellants' have not argued that the claimed shapes yield unexpected results, then the claimed shapes would have been obvious.

Upon the establishment by the Examiner of a prima facie case of obviousness, Appellants can rebut this prima facie case of obviousness by asserting critical or unexpected results<sup>1</sup>. However, the Examiner has failed to establish a prima facie case of obviousness for the limitations recited in each of dependent claims 4, 5 and 8. Thus, Appellants are not required to assert critical or unexpected results, as there is no prima facie case of obviousness to overcome.

Furthermore, although not binding precedent on this Board, Appellants note that in the unpublished opinion of Ex parte Minoru Yoshida et al.<sup>2</sup>, the Board previously addressed the issue regarding a requirement placed on Appellants by the Examiner to show that a particular shape or size is critical. Specifically, the Board wrote:

the examiner takes the position that all claim features regarding particle size, shape and

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<sup>1</sup> Other methods of overcoming a prima facie case of obviousness are, of course, available to Appellants.

<sup>2</sup> (Appeal No. 1996-2593)

relationship between diameter of particle and thickness of thermoplastic layer are satisfied by Murooka in the "absence of a showing of a criticality thereof by appellants" (page 4 of Answer). Here, the examiner has perpetrated clear error by placing the cart before the horse. It is axiomatic that before the burden shifts to an applicant to prove evidence of nonobviousness, such as evidence of criticality or unexpected results, the examiner must establish, in the first instance, that the claimed features would have been prima facie obvious to one of ordinary skill in the art. In the present case, the examiner has made no attempt to establish on this record that the use of aluminum oxide particles having an acicular or platy shape in a polyester composition would have been obvious to one of ordinary skill in the art. In the absence of such a finding by the examiner, appellants are under no burden to demonstrate that the claimed acicular and platy shapes are critical to the claimed invention.

Therefore, for the reasons stated above, Appellants respectfully submit that one having ordinary skill in the art would not have found the limitations recited in each of claims 4, 5 and 8 obviousness within the meaning of 35 U.S.C. § 103 based upon the combination of the Admitted Prior Art in view of Chen.

#### IX. CONCLUSION

It should, therefore, be apparent that the Examiner did not discharge the initial burden of establishing a prima facie case of obviousness under 35 U.S.C. § 103. The Examiner's asserted benefits for modifying the Admitted Prior Art in view of Chen would not have motivated one having ordinary skill in the art to combine the applied prior art in the manner suggested by the Examiner. Furthermore, the Examiner has failed to establish a prima facie case of obviousness for the separate features recited in claims 4, 5 and 8.

#### X. PRAYER FOR RELIEF

Based upon the foregoing, Appellants respectfully submit that one having ordinary skill in the art would not have found the claimed invention obviousness within the meaning of 35 U.S.C. § 103 based upon the Admitted Prior Art in view of Chen. Appellants, therefore,

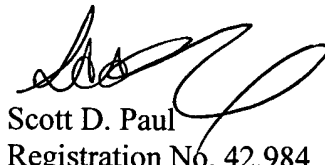
Application No. Application No.: 09/620,718

respectfully solicit the Honorable Board to reverse the Examiner's rejection under 35 U.S.C § 103.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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APPENDIX

1. A semiconductor device having a test mark comprising:  
  
a semiconductor substrate;  
  
a first TEOS layer formed on said semiconductor substrate;  
  
a second TEOS layer formed on said first TEOS layer and having a lower fluidity than that of said first TEOS layer at an elevated temperature;  
  
a recess formed in said first and second TEOS layers and exposing the surface of said semiconductor substrate, wherein the horizontal cross-section of said recess is substantially rectangular in configuration; and  
  
a metal layer formed on said first TEOS layer and opposing a corner of said recess.
2. A semiconductor device according to claim 1, wherein said first TEOS layer contains boron and/or phosphorus.
3. A semiconductor device according to claim 1, wherein said metal layer is a square-shaped layer surround said recess.
4. A semiconductor device according to claim 1, wherein said metal layer is an L-shaped layer surrounding the corner of said recess.
5. A semiconductor device according to claim 1, wherein said metal layer is a delta-shaped layer of which one side opposes to the corner of said recess.

6. A semiconductor device according to claim 1, further comprising an outer metal layer formed outside of said metal layer so that said outer metal layer opposes to the corner of said recess through said metal layer.

7. A semiconductor device according to claim 1, wherein a lower metal layer is embedded in said first TEOS layer which extends between the top and bottom surfaces each neighboring to said semiconductor substrate and said metal layer.

8. A semiconductor device according to claim 7, wherein said lower metal layer consists of a plurality of cylindrical metal layers.